DataSheet

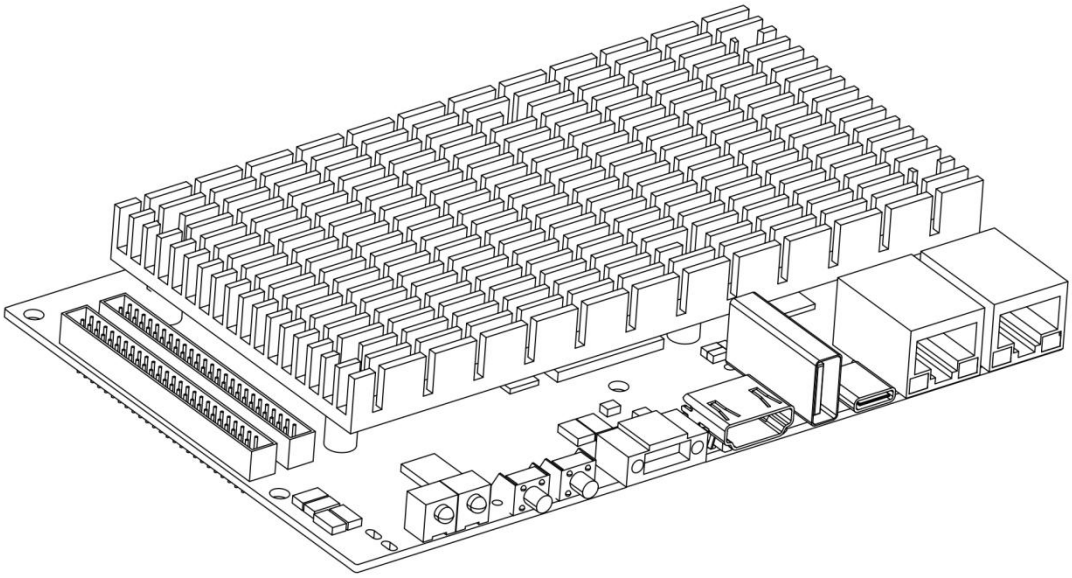
MT-P812

16 AI (16 Bit, 200 kS/s/ch), 4 AO (16 Bit, 125 kS/s/ch), 110 DIO

Singal-Board Controller Device

This document contains the specifications for MT-P812.Specifications are typical at 25°C unless otherwise noted.

Caution Using the MT-P812 in a manner not described in this document may impair the protection the MT-P812 provides.



MANGOTREE

Analog Input

Number of channels	16 single ended
ADC resolution	16 bits
Type of ADC	Successive approximation register (SAR)
Input range	±10V
Input Voltage Ranges	
Measurement Voltage(AI+ to AI-)	
Minimum(V)	±10.2V
Typical(V)	±10.4V
Maximum	±10.6V
Overvoltage protection	±30 V
Conversion time	5 µs minimum
Sample rate	200 kS/s maximum per channel

Table 1. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.142%	±0.070%
	Typical (23 °C ±5 °C)	0.010%	±0.007%

Stability	
Gain drift	4.5 ppm/°C
Offset drift	10 µV/°C
CMRR	120 dB minimum
-3 dB bandwidth	10 kHz
Input impedance	>1 GΩ
Crosstalk	-90 dB
Total Harmonic Distortion(THD)	-107dB
No missing codes	16 bits
DNL	±0.5LSB
INL	±0.5LSB

Analog Output

Number of channels	4
DAC resolution	16 bits
Type of DAC	String
Output voltage range	±10V
Current drive	±10 mA per channel maximum
Output impedance	1 Ω
Sample rate	125 kS/s maximum per channel

Table 2. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.214%	0.075%
	Typical (25 °C, ±5 °C)	0.010%	0.007%

Output voltage drift	5 ppm/°C
Zero-code error drift	±4μV /°C
Protection	
Overvoltage	±30V
Short-circuit	Indefinitely
Noise	
Output noise density	170 uV/ √ Hz
Output noise	50 uVpp
Slew rate	1.8V/us
Crosstalk	76dB
Capacitive drive	1nF
DNL	±1 LSB maximum
INL (endpoint)	±12 LSB maximum

Digital I/O

Table 1. Channel Frequency

Connector	Number of Channels	Voltage Level
Connector J1	80	3.3V
Connector J2	30	5V

Compatibility	LVTTL, LVCMOS
Logic family	Fixed
Voltage level	3.3V/5V

Table 2. Digital Output Logic Levels

Logic Family	Output Low Voltage(VoL) Maximum	Output HighVoltage(VoH) Minimum
3.3V	0.3 V	2.4 V
5V	0.4 V	4.6 V

Maximum DC output current per channel	
Source	4.0 mA
Sink	4.0 mA
Output impedance	50 Ω
Direction control of digital I/O channels	Per Channel
Minimum I/O pulse width	12.5 ns
Minimum sampling period	12.5 ns

Table 3. Digital Input Logic Levels

Logic Family	Input Low Voltage(VIL) Maximum	Input HighVoltage(VIH) Minimum
3.3V	0.8 V	2.0 V
5V	1.5 V	3.5 V

Reconfigurable FPGA

FPGA type	Spartan-6 Lx75
Number of flip-flops	93,296
Number of LUTs	46,648
Embedded Block RAM	3,096 kbits
Number of DSP48 slices	132

Processor

CPU	Intel Z8350
Number of cores	4
CPU frequency	1.92 GHz max
L2 cache	2 MB

Operating System

Supported operating system	Linux RT

Ethernet Port

Numbers of ports	2
Network interface	10Base-T, 100Base-TX

USB Ports

Number of USB 3.0	1
Number of USB 2.0	1

RS-232 Serial Port

Number of Ports	2
Maximum band rate	115,200 bps

Display Port

Supported Port	HDMI

Memory

Processor memory	2 GB DDR3L
Solid-state drive	16 GB Emmc

Maximum Power Requirements

Power requirements are dependent on the digital output loads and configuration of the LabVIEW FPGA VI used in your application.

+12 V	1.2 A

Physical Characteristics

Weight	230 g
Dimensions	153mm*108mm

Safety Voltages

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Shock and Vibration

To meet these specifications, you must panel mount the system.

Operating vibration	
Random (IEC 60068-2-64)	5 g_{rms}, 10 Hz to 500 Hz
Sinusoidal (IEC 60068-2-6)	5 g, 10 Hz to 500 Hz
Operating shock (IEC 60068-2-27) 18 shocks at 6 orientations	30 g, 11 ms half sine; 50 g, 3 ms half sine;

Environmental

Refer to the manual for the chassis you are using for more information about meeting these specifications.

Operating temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 70 °C
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 85 °C
Ingress protection	IP40
Operating humidity (IEC 60068-2-78)	10% RH to 90% RH, noncondensing Storage
humidity (IEC 60068-2-78)	5% RH to 95% RH, noncondensing Pollution
Degree	2
Maximum altitude	4,000 m

Indoor use only.

Support

MT-Master上手指南：

https://server.mangotree.cn:9900/WebFile/Downloads/上手指南/MT-Master/

MT-Master视频教程：

https://server.mangotree.cn:9900/WebFile/Downloads/视频教程/MT-Master/

Master上手指南

Master视频教程

MT-RIO上手指南：

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MT-RIO视频教程：

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RIO上手指南

RIO视频教程

MT-Veristand上手指南：

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MT-Veristand视频教程：

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VeriStand上手指南

VeriStand视频教程

MT-P812 UART Connectivity

	Pin	Signal	Pin	Signal
UART	1	TXD	2	RXD
	3	NC	4	NC
	5	TXD	6	RXD
	7	NC	8	NC
	9	COM	10	COM

MT-P812 正面 50Pin 连接器（J1、J2）引脚定义：

PCB_RIO-J1引脚定义			
功能	引脚		功能
AGND	1	2	AI00
AI08	3	4	AGND
AI09	5	6	AI01
AGND	7	8	AI02
AI10	9	10	AGND
AI11	11	12	AI03
AGND	13	14	AI04
AI12	15	16	AGND
AI13	17	18	AI05
AGND	19	20	AI06
AI14	21	22	AGND
AI15	23	24	AI07
AGND	25	26	AGND
AGND	27	28	AO00
AGND	29	30	AO01
AGND	31	32	AO02
AGND	33	34	AO03
AGND	35	36	NC
AGND	37	38	NC
DGND	39	40	DIO00(5v)
DGND	41	42	DIO01(5v)
DGND	43	44	DIO02(5v)
DGND	45	46	DIO03(5v)
DGND	47	48	DIO04(5v)
DGND	49	50	DIO05(5v)

PCB_RIO-J2引脚定义			
功能	引脚		功能
DGND	1	2	DIO06(5v)
DGND	3	4	DIO07(5v)
DGND	5	6	DIO08(5v)
DGND	7	8	DIO09(5v)
DGND	9	10	DIO10(5v)
DGND	11	12	DIO11(5v)
DGND	13	14	DIO12(5v)
DGND	15	16	DIO13(5v)
DGND	17	18	DIO14(5v)
DGND	19	20	DIO15(5v)
DGND	21	22	DIO16(5v)
DGND	23	24	DIO17(5v)
DGND	25	26	DIO18(5v)
DGND	27	28	DIO19(5v)
DGND	29	30	DIO20(5v)
DGND	31	32	DIO21(5v)
DGND	33	34	DIO22(5v)
DGND	35	36	DIO23(5v)
DGND	37	38	DIO24(5v)
DGND	39	40	DIO25(5v)
DGND	41	42	DIO26(5v)
DGND	43	44	DIO27(5v)
DGND	45	46	DIO28(5v)
DGND	47	48	DIO29(5v)
5V	49	50	5V

MT-P812 背面 100Pin 连接器引脚定义（3.3V DIO）：

PCB_RIO-80 IO引脚定义			
功能	引脚		功能
3V	1	2	3V
DIO00	3	4	DIO10
DIO01	5	6	DIO11
DIO02	7	8	DIO12
DIO03	9	10	DIO13
DIO04	11	12	DIO14
NC	13	14	NC
DIO05	15	16	DIO15
DIO06	17	18	DIO16
DIO07	19	20	DIO17
DIO08	21	22	DIO18
DIO09	23	24	DIO19
DGND	25	26	DGND
DIO20	27	28	DIO30
DIO21	29	30	DIO31
DIO22	31	32	DIO32
DIO23	33	34	DIO33
DIO24	35	36	DIO34
NC	37	38	NC
DIO25	39	40	DIO35
DIO26	41	42	DIO36
DIO27	43	44	DIO37
DIO28	45	46	DIO38
DIO29	47	48	DIO39
DGND	49	50	DGND
DIO40	51	52	DIO50
DIO41	53	54	DIO51
DIO42	55	56	DIO52
DIO43	57	58	DIO53
DIO44	59	60	DIO54
NC	61	62	NC
DIO45	63	64	DIO55
DIO46	65	66	DIO56
DIO47	67	68	DIO57
DIO48	69	70	DIO58
DIO49	71	72	DIO59
DGND	73	74	DGND
DIO60	75	76	DIO70
DIO61	77	78	DIO71
DIO62	79	80	DIO72
DIO63	81	82	DIO73
DIO64	83	84	DIO74
NC	85	86	NC
DIO65	87	88	DIO75
DIO66	89	90	DIO76
DIO67	91	92	DIO77
DIO68	93	94	DIO78
DIO69	95	96	DIO79
5V	97	98	5V
5V	99	100	5V

Dimensions:(mm)