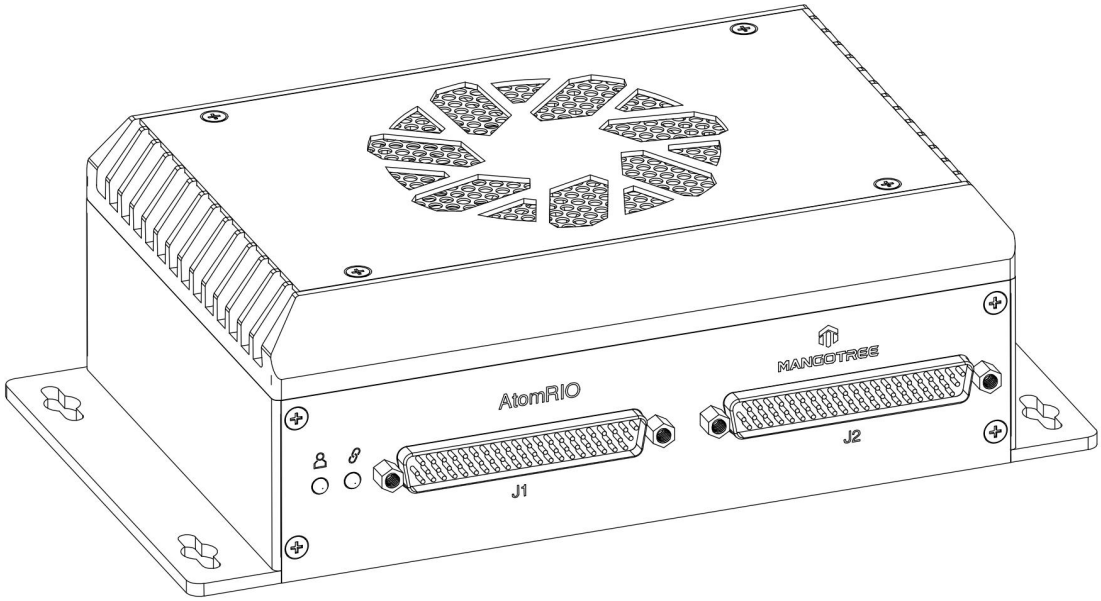
DataSheet

MT-S815

16 AI (16 Bit, 200 kS/s/ch), 8 AO (16 Bit, 125 kS/s/ch),

56 DIO Multifunction Controller Device



This document contains the specifications for MT-S815.Specifications are typical at 25°C unless otherwise noted.

Caution Using the MT-S815 in a manner not described in this document may impair the protection the MT-S815 provides.

MANGOTREE

Analog Input

Number of channels	16 single ended
ADC resolution	16 bits
Type of ADC	Successive approximation register (SAR)
Input range	±10V
Input Voltage Ranges	
Measurement Voltage(AI+ to AI-)	
Minimum(V)	±10.2V
Typical(V)	±10.4V
Maximum	±10.6V
Overvoltage protection	±30 V
Conversion time	5 µs minimum
Sample rate	200 kS/s maximum per channel

Table 1. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.142%	±0.070%
	Typical (23 °C ±5 °C)	0.010%	±0.007%

Stability	
Gain drift	4.5 ppm/°C
Offset drift	10 µV/°C
CMRR	120 dB minimum
-3 dB bandwidth	10 kHz
Input impedance	>1 GΩ
Crosstalk	-90 dB
Total Harmonic Distortion(THD)	-107dB
No missing codes	16 bits
DNL	±0.5LSB
INL	±0.5LSB

Analog Output

Number of channels	8
DAC resolution	16 bits
Type of DAC	String
Output voltage range	±10V
Current drive	±10 mA per channel maximum
Output impedance	1 Ω
Sample rate	125 kS/s maximum per channel

Table 2. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.214%	0.075%
	Typical (25 °C, ±5 °C)	0.010%	0.007%

Output voltage drift	5 ppm/°C
Zero-code error drift	±4µV /°C
Protection	
Overvoltage	±30V
Short-circuit	Indefinitely
Noise	
Output noise density	170 uV/ √ Hz
Output noise	50 uVpp
Slew rate	1.8V/us
Crosstalk	76dB
Capacitive drive	1nF
DNL	±1 LSB maximum
INL (endpoint)	±12 LSB maximum

Digital I/O

Table 3. Number of Channels

Connector	Number of Channels	Voltage Level
Connector J1	16	5V
Connector J2	40	3.3V

Compatibility	LVTTL, LVCMOS
Logic family	Fixed
Voltage level	3.3V/5V

Table 4. Digital Output Logic Levels

Logic Family	Output Low Voltage(VoL) Maximum	Output HighVoltage(VoH) Minimum
3.3V	0.3 V	2.4 V
5V	0.4 V	4.6 V

Output impedance	50 Ω
Direction control of digital I/O channels	Per Channel
Minimum I/O pulse width	12.5 ns
Minimum sampling period	12.5 ns

Table 5. Digital Input Logic Levels

Logic Family	Input Low Voltage(VIL) Maximum	Input HighVoltage(VIH) Minimum
3.3V	0.80 V	2.00 V
5.0V	1.5 V	3.5 V

Reconfigurable FPGA

FPGA type	Spartan-6 Lx75
Number of flip-flops	93,296
Number of LUTs	46,648
Embedded Block RAM	3,096 kbits
Number of DSP48 slices	132

Processor

CPU	I5-1155G7
Number of cores	4 Cores,8 Threads
CPU frequency	4.5 GHz max
Cache	8 MB

Operating System

Supported operating system	Windows10 or Linux RT

Ethernet Port

Numbers of ports	2
Network interface	10Base-T, 100Base-TX, and
	1000Base-T Ethernet

USB Ports

Number of USB 3.0	4

RS-232 Serial Port

Number of Ports	2

Maximum band rate	115,200 bps

Display Port

Supported Port	VGA and HDMI

Memory

Processor memory	4GB DDR4
Solid-state drive	256 GB

Minimum Power Requirements

Power requirements are dependent on the digital output loads and configuration of the LabVIEW FPGA VI used in your application.

+12 V	3 A

Physical Characteristics

Weight	1.2 kg
Dimensions	See end of this document

Safety Voltages

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)

- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Shock and Vibration

To meet these specifications, you must panel mount the system.

Operating vibration	
Random (IEC 60068-2-64)	5 g_{rms}, 10 Hz to 500 Hz
Sinusoidal (IEC 60068-2-6)	5 g, 10 Hz to 500 Hz
Operating shock (IEC 60068-2-27)	30 g, 11 ms half sine; 50 g, 3 ms half sine; 18 shocks at 6 orientations

Environmental

Refer to the manual for the chassis you are using for more information about meeting these specifications.

Operating temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 70 °C
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 85 °C
Ingress protection	IP40
Operating humidity (IEC 60068-2-78)	10% RH to 90% RH, noncondensing Storage
humidity (IEC 60068-2-78)	5% RH to 95% RH, noncondensing Pollution
Degree	2
Maximum altitude	4,000 m

Indoor use only.

Support

MT-Master上手指南：

https://server.mangotree.cn:9900/WebFile/Downloads/上手指南/MT-Master/

MT-Master视频教程：

https://server.mangotree.cn:9900/WebFile/Downloads/视频教程/MT-Master/

Master上手指南

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RIO上手指南

RIO视频教程

MT-Veristand上手指南：

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MT-Veristand视频教程：

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VeriStand上手指南

VeriStand视频教程

MT-S815 Pinout

Connector J1					
Pin	Definition	Pin	Definition	Pin	Definition
1	5V	22	AGND	43	AI 15
2	5V	23	AO 0	44	NC
3	DGND	24	AO 1	45	DIO 0
4	DGND	25	AGND	46	DIO 1
5	AI 0	26	AGND	47	DIO 2
6	NC	27	AO 2	48	DIO 3
7	AI 1	28	AO 3	49	DIO 4
8	NC	29	AI 8	50	DIO 5
9	AI 2	30	AO 4	51	DIO 6
10	NC	31	AI 9	52	DIO 7
11	AI 3	32	AO 5	53	DIO 8
12	NC	33	AI 10	54	DIO 9
13	AI 4	34	AO 6	55	DIO 10
14	NC	35	AI 11	56	DIO 11
15	AI 5	36	AO 7	57	DIO 12
16	NC	37	AI 12	58	DIO 13
17	AI 6	38	NC	59	DIO 14
18	NC	39	AI 13	60	DIO 15
19	AI 7	40	NC	61	DGND
20	NC	41	AI 14	62	DGND
21	AGND	42	NC		

Note: The voltage level of digital signals is 5V in connector J1.

Connector J2					
Pin	Definition	Pin	Definition	Pin	Definition
1	5V	22	DIO 17	43	DIO 36
2	5V	23	DIO 18	44	DIO 37
3	DGND	24	DIO 19	45	DIO 38
4	DGND	25	DGND	46	DIO 39
5	DIO 0	26	DGND	47	DGND
6	DIO 1	27	DIO 20	48	DGND
7	DIO 2	28	DIO 21	49	3.3V
8	DIO 3	29	DIO 22	50	3.3V
9	DIO 4	30	DIO 23	51	DGND
10	DIO 5	31	DIO 24	52	DGND
11	DIO 6	32	DIO 25	53	DGND
12	DIO 7	33	DIO 26	54	DGND
13	DIO 8	34	DIO 27	55	DGND
14	DIO 9	35	DIO 28	56	DGND
15	DIO 10	36	DIO 29	57	DGND
16	DIO 11	37	DIO 30	58	DGND
17	DIO 12	38	DIO 31	59	DGND
18	DIO 13	39	DIO 32	60	DGND
19	DIO 14	40	DIO 33	61	DGND
20	DIO 15	41	DIO 34	62	DGND
21	DIO 16	42	DIO 35		

Note: The voltage level of digital signals is 3.3V in connector J2.

Dimensions:(mm)