

DataSheet

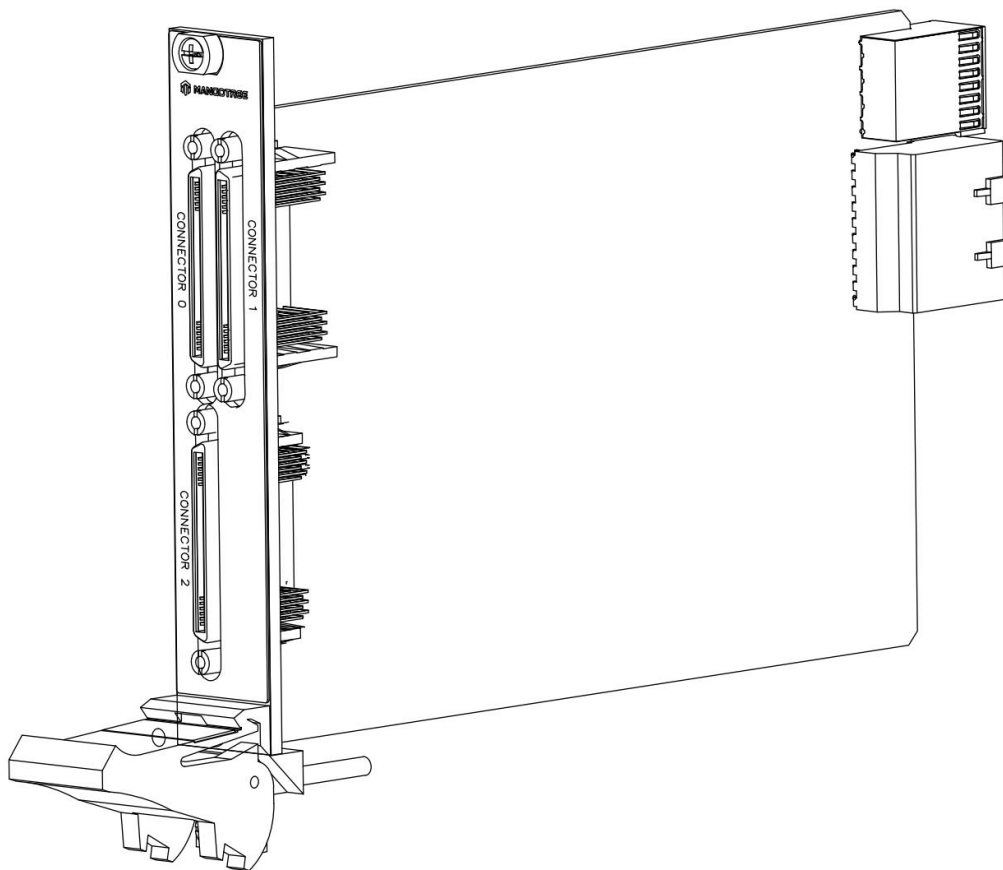
# MT-X921

R Series Reconfigurable I/O Module(AI,AO,DIO),24 AI, 8 AO,  
64 DIO, 1MS/s AIO, Kintex-7 325T FPGA

This document contains the specifications for MT-X921.Specifications are typical at 25°C unless otherwise noted.



**Caution** Using the MT-X921 in a manner not described in this document may impair the protection the MT-X921 provides.



# Analog Input

Number of channels	24
ADC resolution	16 bits
Type of ADC	Successive approximation register (SAR)
Input range	$\pm 10\text{V}$
Input Voltage Ranges	
Measurement Voltage(AI+ to AI-)	
Minimum(V)	$\pm 10.2\text{V}$
Typical(V)	$\pm 10.4\text{V}$
Maximum	$\pm 10.6\text{V}$
Overvoltage protection	$\pm 30\text{ V}$
Conversion time	1 $\mu\text{s}$ minimum
Sample rate	1 MS/s maximum per channel

**Table 1.** Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.142%	$\pm 0.070\%$
	Typical (23 °C $\pm 5$ °C)	0.010%	$\pm 0.007\%$

CMRR	120 dB minimum
-3 dB bandwidth	>15 kHz
Input impedance	1M $\Omega$
Crosstalk	-90 dB
Total Harmonic Distortion(THD)	-107dB
No missing codes	16 bits
DNL	$\pm 0.4\text{LSB}$
INL	$\pm 0.5\text{LSB}$
SNR	90 dB

## Analog Output

Number of channels	8
DAC resolution	16 bits
Type of DAC	String
Output voltage range	$\pm 10\text{V}$
Current drive	$\pm 10\text{ mA}$ per channel maximum
Output impedance	$375\ \Omega$
Sample rate	1 MS/s maximum per channel

**Table 2.** Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.214%	0.075%
	Typical (25 °C, $\pm 5\text{ °C}$ )	0.010%	0.007%

Gain drift	$\pm 0.1\text{ ppm}/^\circ\text{C}$
Zero-code drift	$\pm 0.05\text{ ppm}/^\circ\text{C}$
Protection	
Overvoltage	$\pm 30\text{V}$
Short-circuit	Indefinitely
Noise	
Output noise	$10\text{nV} / \sqrt{\text{Hz}}$
Slew rate	$25\text{V}/\mu\text{s}$
Crosstalk	74dB
Capacitive drive	1nF
DNL	$\pm 1\text{ LSB}$ maximum
INL (endpoint)	$\pm 1\text{ LSB}$ maximum

# Digital I/O

---

**Table 3.** Channel Frequency

Connector	Number of Channels	Maximum Frequency
Connector 0	16	80 MHz
Connector 1	16	80 MHz
Connector 2	32	80 MHz

---

Compatibility LVTTL, LVCOMS

---

Logic family Fixed

---

Voltage level 3.3V

---

**Table 4.** Digital Output Logic Levels

Logic Family	Current	Output Low Voltage(VoL)	Output High Voltage(VoH)
		Maximum	Maximum
3.3V	100uA	0.20 V	3.00 V
	4mA	0.40 V	2.40 V

Maximum DC output current per channel

---

Source 4.0 mA

---

Sink 4.0 mA

---

Output impedance 50  $\Omega$

---

Direction control of digital I/O channels Per Channel

---

Minimum I/O pulse width 6.25 ns

---

Minimum sampling period 5 ns

---

**Table 5.** Digital Input Logic Levels

Logic Family	Input Low Voltage(VIL)	Input High Voltage(VIH)
	Maximum	Maximum
3.3V	0.80 V	2.00 V

Minimum input	-0.3 V
Maximum input	3.6V
Input leakage current	± 15uA maximum
Input impedance	50kΩ typical, pull-down

## Reconfigurable FPGA

FPGA type	Kintex-7 325T
Number of flip-flops	407,600
Number of LUTs	203,800
Embedded Block RAM	16,020 kbits
Number of DSP48 slices	840

## Maximum Power Requirements

Power requirements are dependent on the digital output loads and configuration of the LabVIEW FPGA VI used in your application.

+3.3V	3 A
+12 V	2 A

## Safety Voltages

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

## CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

## Shock and Vibration

To meet these specifications, you must panel mount the system.

### Operating vibration

Random (IEC 60068-2-64)	5 g <sub>rms</sub> , 10 Hz to 500 Hz
Sinusoidal (IEC 60068-2-6)	5 g, 10 Hz to 500 Hz
Operating shock (IEC 60068-2-27)	30 g, 11 ms half sine; 50 g, 3 ms half sine; 18 shocks at 6 orientations

## Environmental

Refer to the manual for the chassis you are using for more information about meeting these specifications.

Operating temperature	-40 °C to 70 °C (IEC 60068-2-1, IEC 60068-2-2)
Storage temperature	-40 °C to 85 °C (IEC 60068-2-1, IEC 60068-2-2)
Ingress protection	IP40
Operating humidity (IEC 60068-2-78)	10% RH to 90% RH, noncondensing Storage
humidity (IEC 60068-2-78)	5% RH to 95% RH, noncondensing Pollution
Degree	2
Maximum altitude	4,000 m

Indoor use only.

# Support

MT-Master上手指南:

<https://server.mangotree.cn:9900/WebFile/Downloads/上手指南/MT-Master/>

MT-Master视频教程:

<https://server.mangotree.cn:9900/WebFile/Downloads/视频教程/MT-Master/>



Master上手指南



Master视频教程

MT-RIO上手指南:

<https://server.mangotree.cn:9900/WebFile/Downloads/上手指南/MT-RIO/>

MT-RIO视频教程:

<https://server.mangotree.cn:9900/WebFile/Downloads/视频教程/MT-RIO/>



RIO上手指南



RIO视频教程

MT-Veristand上手指南:

<https://server.mangotree.cn:9900/WebFile/Downloads/上手指南/MT-VeriStand/>

MT-Veristand视频教程:

<https://server.mangotree.cn:9900/WebFile/Downloads/视频教程/MT-VeriStand/>



VeriStand上手指南

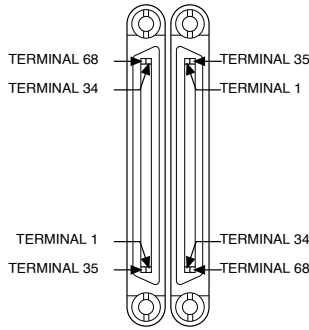


VeriStand视频教程

# MT-X921 Pinout

CONNECTOR 0

AI 0+	68	34	AI 0-
A GND	67	33	A GND
AI 1+	66	32	AI 1-
AI 2+	65	31	AI 2-
A GND	64	30	A GND
AI 3+	63	29	AI 3-
AI 4+	62	28	AI 4-
A GND	61	27	A GND
AI 5+	60	26	AI 5-
AI 6+	59	25	AI 6-
A GND	58	24	A GND
AI 7+	57	23	AI 7-
NC	56	22	NC
AO 0	55	21	A GND
AO 1	54	20	A GND
AO 2	53	19	A GND
AO 3	52	18	A GND
AO 4	51	17	A GND
AO 5	50	16	A GND
AO 6	49	15	A GND
AO 7	48	14	A GND
DIO 15	47	13	DIO 14
DIO 13	46	12	DIO 12
DIO 11	45	11	DIO 10
DIO 9	44	10	DIO 8
DIO 7	43	9	D GND
DIO 6	42	8	D GND
DIO 5	41	7	D GND
DIO 4	40	6	D GND
DIO 3	39	5	D GND
DIO 2	38	4	D GND
DIO 1	37	3	D GND
DIO 0	36	2	D GND
+5 V	35	1	+5 V



NC = No Connect

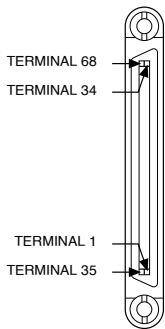
CONNECTOR 1

+5 V	1	35	+5 V
D GND	2	36	DIO 0
D GND	3	37	DIO 1
D GND	4	38	DIO 2
D GND	5	39	DIO 3
D GND	6	40	DIO 4
D GND	7	41	DIO 5
D GND	8	42	DIO 6
D GND	9	43	DIO 7
DIO 8	10	44	DIO 9
DIO 10	11	45	DIO 11
DIO 12	12	46	DIO 13
DIO 14	13	47	DIO 15
AI 23-	14	48	AI 23+
AI 22-	15	49	AI 22+
AI 21-	16	50	AI 21+
AI 20-	17	51	AI 20+
AI 19-	18	52	AI 19+
AI 18-	19	53	AI 18+
AI 17-	20	54	AI 17+
AI 16-	21	55	AI 16+
A GND	22	56	A GND
AI 15-	23	57	AI 15+
A GND	24	58	A GND
AI 14-	25	59	AI 14+
AI 13-	26	60	AI 13+
A GND	27	61	A GND
AI 12-	28	62	AI 12+
AI 11-	29	63	AI 11+
A GND	30	64	A GND
AI 10-	31	65	AI 10+
AI 9-	32	66	AI 9+
A GND	33	67	A GND
AI 8-	34	68	AI 8+

NC = No Connect

CONNECTOR 2

D GND	68	34	D GND
NC	67	33	D GND
D GND	66	32	D GND
DIO 0	65	31	DIO 1
D GND	64	30	D GND
DIO 2	63	29	DIO 3
D GND	62	28	D GND
DIO 4	61	27	DIO 5
D GND	60	26	D GND
DIO 6	59	25	DIO 7
D GND	58	24	D GND
DIO 8	57	23	DIO 9
D GND	56	22	D GND
DIO 10	55	21	DIO 11
D GND	54	20	D GND
DIO 12	53	19	DIO 13
D GND	52	18	D GND
DIO 14	51	17	DIO 15
D GND	50	16	D GND
DIO 16	49	15	DIO 17
D GND	48	14	D GND
DIO 18	47	13	DIO 19
D GND	46	12	D GND
DIO 20	45	11	DIO 21
D GND	44	10	D GND
DIO 22	43	9	DIO 23
D GND	42	8	D GND
DIO 24	41	7	DIO 25
D GND	40	6	D GND
DIO 26	39	5	DIO 27
D GND	38	4	D GND
DIO 28	37	3	DIO 29
D GND	36	2	D GND
DIO 30	35	1	DIO 31



NC = No Connect



Dimensions:(mm)

