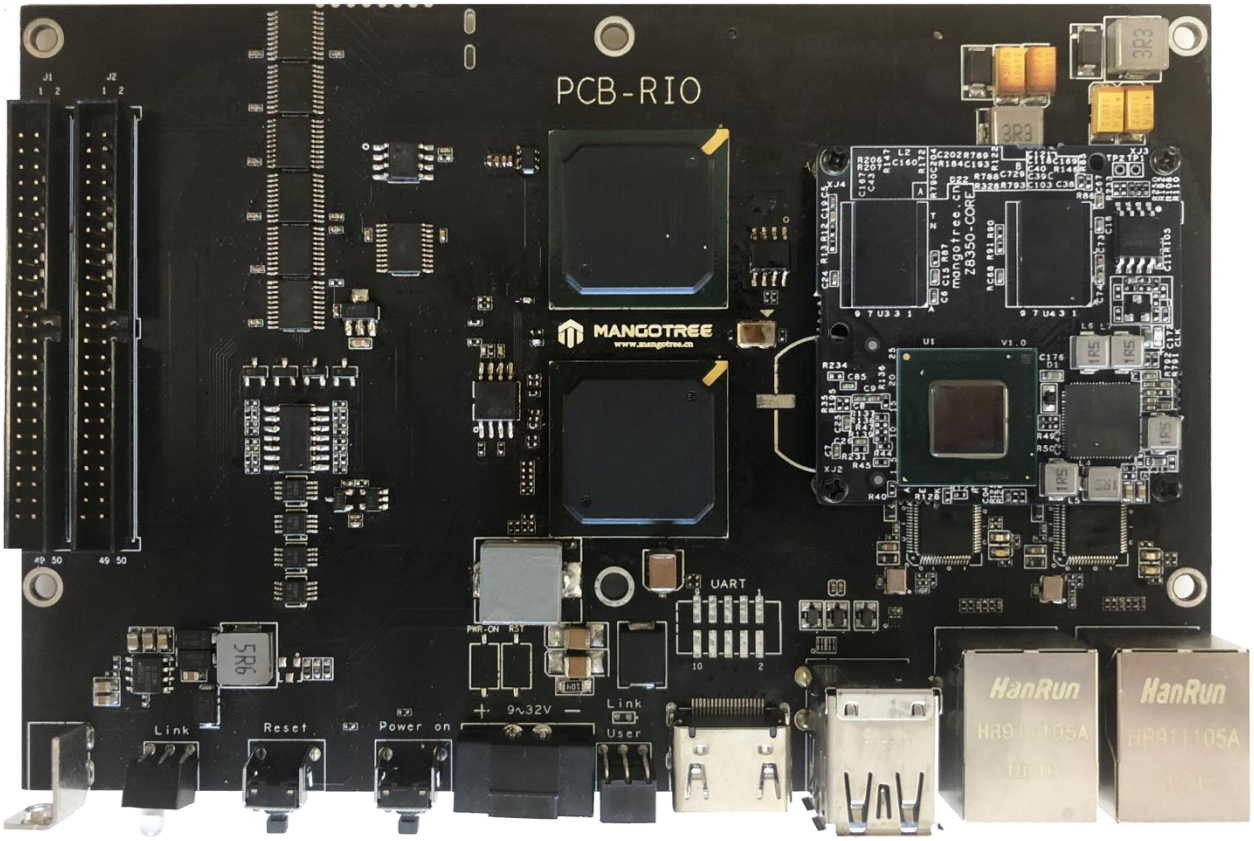
SPECIFICATIONS

MT P812

16 AI (16 Bit, 200 kS/s/ch), 4 AO (16 Bit, 125 kS/s/ch), 110 DIO

Singal-Board Controller Device



This document contains the specifications for MT P812.Specifications are typical at 25°C unless otherwise noted.

Caution Using the MT P812 in a manner not described in this document may impair the protection the MT P812 provides.

MANGOTREE

Analog Input

Number of channels	16 single ended
ADC resolution	16 bits
Type of ADC	Successive approximation register (SAR)
Input range	±10V
Input Voltage Ranges	
Measurement Voltage(AI+ to AI-)	
Minimum(V)	±10.2V
Typical(V)	±10.4V
Maximum	±10.6V
Overvoltage protection	±30 V
Conversion time	5 μs minimum
Sample rate	200 kS/s maximum per channel

Table 1. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.142%	±0.070%
	Typical (23 °C ±5 °C)	0.010%	±0.007%

Stability	
Gain drift	4.5 ppm/°C
Offset drift	10 μV/°C
CMRR	120 dB minimum
-3 dB bandwidth	>100 kHz
Input impedance	>1 GΩ
Crosstalk	-90 dB
Total Harmonic Distortion(THD)	-107dB
No missing codes	16 bits
DNL	±0.5LSB
INL	±0.5LSB

Analog Output

Number of channels	4
DAC resolution	16 bits
Type of DAC	String
Output voltage range	±10V
Current drive	±10 mA per channel maximum
Output impedance	1 Ω
Sample rate	125 kS/s maximum per channel

Table 2. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.214%	0.075%
	Typical (25 °C, ±5 °C)	0.010%	0.007%

Output voltage drift	5 ppm/°C
Zero-code error drift	±4μV /°C
Protection	
Overvoltage	±30V
Short-circuit	Indefinitely
Noise	
Output noise density	170 uV/ √ Hz
Output noise	50 uVpp
Slew rate	1.8V/us
Crosstalk	76dB
Capacitive drive	1nF
DNL	±1 LSB maximum
INL (endpoint)	±12 LSB maximum

Digital I/O

Table 1. Channel Frequency

Connector	Number of Channels	Voltage Level
Connector J1	80	3.3V
Connector J2	30	5V

Compatibility	LVTTL, LVCMOS
Logic family	Fixed
Voltage level	3.3V/5V

Table 2. Digital Output Logic Levels

Logic Family	Output Low Voltage(VoL) Maximum	Output HighVoltage(VoH) Minimum
3.3V	0.3 V	2.4 V
5V	0.4 V	4.6 V

Maximum DC output current per channel	
Source	4.0 mA
Sink	4.0 mA
Output impedance	50 Ω
Direction control of digital I/O channels	Per Channel
Minimum I/O pulse width	12.5 ns
Minimum sampling period	12.5 ns

Table 3. Digital Input Logic Levels

Logic Family	Input Low Voltage(VIL) Maximum	Input HighVoltage(VIH) Minimum
3.3V	0.8 V	2.0 V
5V	1.5 V	3.5 V

Reconfigurable FPGA

FPGA type	Spartan-6 Lx75
Number of flip-flops	93,296
Number of LUTs	46,648
Embedded Block RAM	3,096 kbits
Number of DSP48 slices	132

Processor

CPU	Intel Z8350
Number of cores	4
CPU frequency	1.92 GHz max
L2 cache	2 MB

Operating System

Supported operating system	Linux RT

Ethernet Port

Numbers of ports	2
Network interface	10Base-T, 100Base-TX

USB Ports

Number of USB 3.0	1
Number of USB 2.0	1

RS-232 Serial Port

Number of Ports	2

Maximum band rate	115,200 bps

Display Port

Supported Port	HDMI

Memory

Processor memory	2 GB DDR3L
Solid-state drive	16 GB Emmc

Maximum Power Requirements

Power requirements are dependent on the digital output loads and configuration of the LabVIEW FPGA VI used in your application.

+12 V	1.2 A

Physical Characteristics

Weight	230 g
Dimensions	153mm*108mm

Safety Voltages

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)

- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Shock and Vibration

To meet these specifications, you must panel mount the system.

Operating vibration	
Random (IEC 60068-2-64)	5 g_{rms}, 10 Hz to 500 Hz
Sinusoidal (IEC 60068-2-6)	5 g, 10 Hz to 500 Hz
Operating shock (IEC 60068-2-27) 18 shocks at 6 orientations	30 g, 11 ms half sine; 50 g, 3 ms half sine;

Environmental

Refer to the manual for the chassis you are using for more information about meeting these specifications.

Operating temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 70 °C
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 85 °C
Ingress protection	IP40
Operating humidity (IEC 60068-2-78)	10% RH to 90% RH, noncondensing Storage
humidity (IEC 60068-2-78)	5% RH to 95% RH, noncondensing Pollution
Degree	2
Maximum altitude	4,000 m

Indoor use only.