

SPECIFICATIONS

MT PXIe-6502

R Series Reconfigurable I/O Module(AI,AO,DIO),8 AI, 24 AO,
64 DIO, 1MS/s AIO, Kintex-7 325T FPGA

This document contains the specifications for MT PXIe-6301.Specifications are typical at 25°C unless otherwise noted.



Caution Using the MT PXIe-6301 in a manner not described in this document may impair the protection the MT PXIe-6301 provides.

Analog Input

Number of channels	8
ADC resolution	16 bits
Type of ADC	Successive approximation register (SAR)
Input range	$\pm 10V$
Input Voltage Ranges	
Measurement Voltage(AI+ to AI-)	
Minimum(V)	$\pm 10.2V$
Typical(V)	$\pm 10.4V$
Maximum	$\pm 10.6V$
Overvoltage protection	$\pm 30 V$
Conversion time	1 μs minimum
Sample rate	1 MS/s maximum per channel

Table 1. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.142%	±0.070%
	Typical (23 °C ±5 °C)	0.010%	±0.007%

CMRR	120 dB minimum
------	----------------

-3 dB bandwidth	>15 kHz
-----------------	---------

Input impedance	1MΩ
-----------------	-----

Crosstalk	-90 dB
-----------	--------

Total Harmonic Distortion(THD)	-107dB
--------------------------------	--------

No missing codes	16 bits
------------------	---------

DNL	±0.4LSB
-----	---------

INL	±0.5LSB
-----	---------

SNR	90 dB
-----	-------

SFDR	109 dB
------	--------

Analog Output

Number of channels	24
--------------------	----

DAC resolution	16 bits
----------------	---------

Type of DAC	String
-------------	--------

Output voltage range	±10V
----------------------	------

Current drive	±10 mA per channel maximum
---------------	----------------------------

Output impedance	375 Ω
------------------	-------

Sample rate	1 MS/s maximum per channel
-------------	----------------------------

Table 2. Accuracy

Measurement Conditions		Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Calibrated	Maximum (-40 °C to 70 °C)	0.214%	0.075%
	Typical (25 °C, ±5 °C)	0.010%	0.007%

Gain drift	±0.1 ppm/°C
Zero-code drift	±0.05 ppm/°C
Protection	
Overvoltage	±30V
Short-circuit	Indefinitely
Noise	
Output noise	10nV / √Hz
Slew rate	25V/μs
Crosstalk	74dB
Capacitive drive	1nF
DNL	±1 LSB maximum
INL (endpoint)	±1 LSB maximum

Digital I/O

Table 3. Channel Frequency

Connector	Number of Channels	Maximum Frequency
Connector 0	16	80 MHz
Connector 1	16	80 MHz
Connector 2	32	80 MHz

Compatibility	LVTTL, LVCOMS
Logic family	Fixed
Voltage level	3.3V

Table 4. Digital Output Logic Levels

Logic Family	Current	Output Low Voltage(VoL) Maximum	Output High Voltage(VoH) Maximum
3.3V	100uA	0.20 V	3.00 V
	4mA	0.40 V	2.40 V

Maximum DC output current per channel

Source	4.0 mA
Sink	4.0 mA
Output impedance	50 Ω
Direction control of digital I/O channels	Per Channel
Minimum I/O pulse width	6.25 ns
Minimum sampling period	5 ns

Table 5. Digital Input Logic Levels

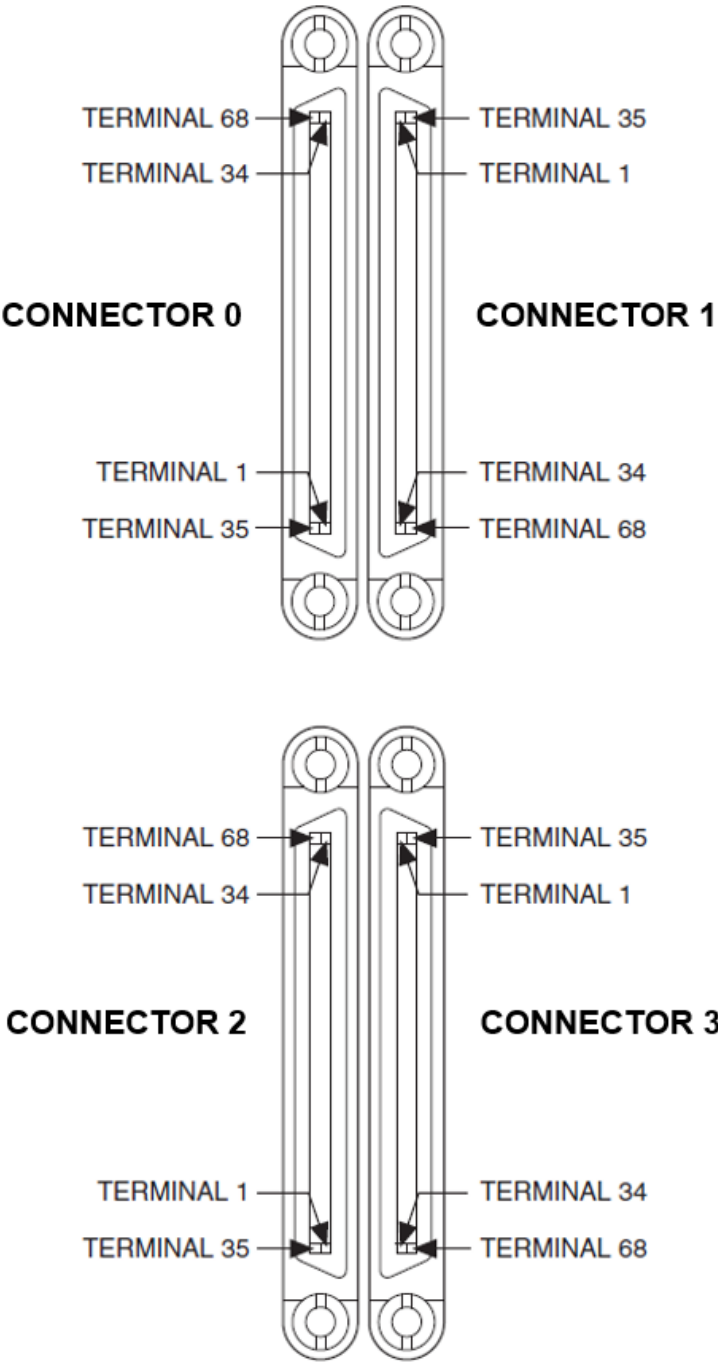
Logic Family	Input Low Voltage(VIL) Maximum	Input High Voltage(VIH) Maximum
3.3V	0.80 V	2.00 V

Minimum input	-0.3 V
Maximum input	3.6V
Input leakage current	$\pm 15\mu\text{A}$ maximum
Input impedance	50k Ω typical, pull-down

Reconfigurable FPGA

FPGA type	Kintex-7 325T
Number of flip-flops	407,600
Number of LUTs	203,800
Embedded Block RAM	16,020 kbits
Number of DSP48 slices	840

Pinouts



CONNECTOR 0

AI0+	68	34	AI0-
AIGND	67	33	AIGND
AI1+	66	32	AI1-
AI2+	65	31	AI2-
AIGND	64	30	AIGND
AI3+	63	29	AI3-
AI4+	62	28	AI4-
AIGND	61	27	AIGND
AI5+	60	26	AI5-
AI6+	59	25	AI6-
AIGND	58	24	AIGND
AI7+	57	23	AI7-
NC	56	22	NC
AO0	55	21	AOGND
AO1	54	20	AOGND
AO2	53	19	AOGND
AO3	52	18	AOGND
AO4	51	17	AOGND
AO5	50	16	AOGND
AO6	49	15	AOGND
AO7	48	14	AOGND
DIO15	47	13	DIO14
DIO13	46	12	DIO12
DIO11	45	11	DIO10
DIO9	44	10	DIO8
DIO7	43	9	DGND
DIO6	42	8	DGND
DIO5	41	7	DGND
DIO4	40	6	DGND
DIO3	39	5	DGND
DIO2	38	4	DGND
DIO1	37	3	DGND
DIO0	36	2	DGND
+5V	35	1	+5V

CONNECTOR 1

AO8	68	34	AOGND
AOGND	67	33	AOGND
AO9	66	32	AOGND
AO10	65	31	AOGND
AOGND	64	30	AOGND
AO11	63	29	AOGND
AO12	62	28	AOGND
AOGND	61	27	AOGND
AO13	60	26	AOGND
AO14	59	25	AOGND
AOGND	58	24	AOGND
AO15	57	23	AOGND
NC	56	22	NC
AO16	55	21	AOGND
AO17	54	20	AOGND
AO18	53	19	AOGND
AO19	52	18	AOGND
AO20	51	17	AOGND
AO21	50	16	AOGND
AO22	49	15	AOGND
AO23	48	14	AOGND
DIO15	47	13	DIO14
DIO13	46	12	DIO12
DIO11	45	11	DIO10
DIO9	44	10	DIO8
DIO7	43	9	DGND
DIO6	42	8	DGND
DIO5	41	7	DGND
DIO4	40	6	DGND
DIO3	39	5	DGND
DIO2	38	4	DGND
DIO1	37	3	DGND
DIO0	36	2	DGND
+5V	35	1	+5V

CONNECTOR 2

DGND	68	34	DGND
NC	67	33	DGND
DGND	66	32	DGND
DIO0	65	31	DIO1
DGND	64	30	DGND
DIO2	63	29	DIO3
DGND	62	28	DGND
DIO4	61	27	DIO5
DGND	60	26	DGND
DIO6	59	25	DIO7
DGND	58	24	DGND
DIO8	57	23	DIO9
DGND	56	22	DGND
DIO10	55	21	DIO11
DGND	54	20	DGND
DIO12	53	19	DIO13
DGND	52	18	DGND
DIO14	51	17	DIO15
DGND	50	16	DGND
DIO16	49	15	DIO17
DGND	48	14	DGND
DIO18	47	13	DIO19
DGND	46	12	DGND
DIO20	45	11	DIO21
DGND	44	10	DGND
DIO22	43	9	DIO23
DGND	42	8	DGND
DIO24	41	7	DIO25
DGND	40	6	DGND
DIO26	39	5	DIO27
DGND	38	4	DGND
DIO28	37	3	DIO29
DGND	36	2	DGND
DIO30	35	1	DIO31

CONNECTOR 3

NC	68	34	NC
NC	67	33	NC
NC	66	32	NC
NC	65	31	NC
NC	64	30	NC
NC	63	29	NC
NC	62	28	NC
NC	61	27	NC
NC	60	26	NC
NC	59	25	NC
NC	58	24	NC
NC	57	23	NC
NC	56	22	NC
NC	55	21	NC
NC	54	20	NC
NC	53	19	NC
NC	52	18	NC
NC	51	17	NC
NC	50	16	NC
NC	49	15	NC
NC	48	14	NC
NC	47	13	NC
NC	46	12	NC
NC	45	11	NC
NC	44	10	NC
NC	43	9	NC
NC	42	8	NC
NC	41	7	NC
NC	40	6	NC
NC	39	5	NC
NC	38	4	NC
NC	37	3	NC
NC	36	2	NC
NC	35	1	NC

Maximum Power Requirements

Power requirements are dependent on the digital output loads and configuration of the LabVIEW FPGA VI used in your application.

+3.3 V 3 A

+12 V 2 A

Safety Voltages

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Shock and Vibration

To meet these specifications, you must panel mount the system.

Operating vibration

Random (IEC 60068-2-64)	5 g _{rms} , 10 Hz to 500 Hz
Sinusoidal (IEC 60068-2-6)	5 g, 10 Hz to 500 Hz
Operating shock (IEC 60068-2-27)	30 g, 11 ms half sine; 50 g, 3 ms half sine; 18 shocks at 6 orientations

Environmental

Refer to the manual for the chassis you are using for more information about meeting these specifications.

Operating temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 70 °C
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 °C to 85 °C
Ingress protection	IP40
Operating humidity (IEC 60068-2-78)	10% RH to 90% RH, noncondensing Storage
humidity (IEC 60068-2-78)	5% RH to 95% RH, noncondensing Pollution
Degree	2
Maximum altitude	4,000 m

Indoor use only.